Abstract of the Disclosure:

An oversampling clock recovery method according to this invention generates non-uniform three-phase clock signals CLKa, CLKb, and CLKc having non-uniform intervals for one bit of an input data i and controls phases of the clock signals so that either phase of two edges of two-phase clock signals CLKb and CLKc having a relatively narrower interval of 57ps synchronizes with a phase of a transition point of the input data i. By changing clock signals to be phase-locked in three delay locked loops (DLLs), a phase interval of 57ps is formed.